Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1. (Canceled)

2. (Currently Amended) A semiconductor circuit ~~according to claim 1,~~ comprising:

a first voltage relaxation circuit coupled between first and second nodes, the first node receiving a first potential;

a second voltage relaxation circuit coupled between third and fourth nodes, the third node receiving said first potential;

a first charge pump circuit with an output thereof coupled to the second node;

a second charge pump circuit with an output thereof coupled to the fourth node;

a third charge pump circuit with an output thereof coupled to the first charge pump;

a fourth charge pump circuit with an output thereof coupled to the second charge pump;

a first rectifier MOSFET with a source-drain path thereof coupled between the second node and a fifth node; and

a second rectifier MOSFET with a source-drain path thereof coupled between the fourth node and said fifth node.

wherein the first charge pump circuit outputs a first signal which varies between a high level and a low level alternately and periodically,

wherein the second charge pump circuit outputs a second signal which varies between a high level and a low level alternately and periodically, the high level of the second signal being equal to the high level of the first signal,

wherein the third charge pump circuit outputs a third signal which varies between a high level and a low level alternately and periodically, the high level of the third signal being lower than the high level of the first signal,

wherein the fourth charge pump circuit outputs a fourth signal which varies between a high level and a low level alternately and periodically, the high level of the fourth signal being equal to the high level of the third signal,

wherein the first voltage relaxation circuit comprises first and second MOSFETs having their source-drain paths coupled in series between the first and second nodes, and

wherein the second voltage relaxation circuit comprises third and fourth MOSFETs having their source-drain paths coupled in series between the third and fourth nodes.

3. (Original) A semiconductor circuit according to claim 2,

wherein the first and second MOSFETs have the same channel conductivity type, and wherein the third and fourth MOSFETs have the same channel conductivity type.

4. (Original) A semiconductor circuit according to claim 2,

wherein the gate of the first rectifier MOSFET is coupled to the second charge pump circuit,

wherein the gate of the second rectifier MOSFET is coupled to the first charge pump circuit, and

wherein the gates of the first and second rectifier MOSFETs receive a complementary voltage.

5. (Original) A semiconductor circuit according to claim 4,

wherein a gate of the first MOSFET is controlled by a fifth signal,

wherein a gate of the third MOSFET is controlled by a sixth signal, and

wherein gates of the second and fourth MOSFETs are commonly coupled.

6. (Original) A semiconductor circuit according to claim 4,

wherein the high level of the first and second signals, respectively, is three times the magnitude of the first potential, and

wherein the high level of the third and fourth signals, respectively, is twice the magnitude of the first potential.

7. (Original) A semiconductor circuit according to claim 4,

wherein the first and second rectifier MOSFETs have the same conductivity type, and

wherein the first MOSFET has a different conductivity type from the first rectifier MOSFET.

8. (Original) A semiconductor circuit according to claim 4, further comprising:

a plurality of word lines, a plurality of bit lines, and a plurality of memory cells coupled to the plurality of word lines and bit lines; and

a row decoder for selecting ones of said plurality of word lines,

wherein said row decoder receives a voltage corresponding to the output of the first and second rectifier MOSFETs.

9. (Original) A semiconductor circuit according to claim 8,

wherein said plurality of memory cells are dynamic random access memory (DRAM) cells.

10. (Original) A semiconductor circuit according to claim 4,

wherein when the first signal is at said high level, the second signal is at said low level, and when the first signal is at said low level, the second signal is at said high level.

11. (Original) A semiconductor circuit according to claim 2,

wherein said first through fourth MOSFETs have the same channel conductivity type, and

wherein the first and second rectifier MOSFETs have a channel conductivity type opposite that of the first through fourth MOSFETs, respectively.

Claims 12-20. (Canceled)